AMENDMENTS TO THE CLAIMS

Claims 1 - 54. (Cancelled)

Claim 55. (Previously Presented)

A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a bottom spacer;

layering a top spacer;

layering a top injector adjacent to the bottom injector, the bottom injector and top injector layers forming a p-i-n junction; and

layering a material between the bottom injector and top spacers which serves as a tunnel barrier, wherein the bottom injector layer, the top injector layer, and said material form a p-i-n junction, where i represents at least one material provided between the bottom injector and the top injector.

Claims 56-57. (Cancelled)

Claim 58. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claim ~~54,~~ 55, ~~56, or 57,~~ wherein the layers in the interband tunnel diode are grown epitaxially.

Claim 59. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claim ~~54,~~ 55, ~~56, or 57~~, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are a semiconductor or insulator.

Claim 60. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claim ~~54,~~ 55, ~~56, or 57,~~ wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are comprised of a Group IV alloy.

Claim 61. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims ~~54,~~ 55, ~~56, or 57,~~ wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are comprised of, but not limited to, Si, Ge, C, Sn, Si1-xGex, Si1-xCx, Si1-xSnx, Si1-x-yGexCy, Si1-x-y-zGexCySnz, Sil-xOx, Si1-xNx, A11-xOx, or combinations thereof.

Claim 62. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims ~~54,~~ 55, ~~56, or 57,~~ wherein the layers in the interband tunnel diode are grown in a molecular beam epitaxial (MBE) growth system.

Claim 63. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims ~~54,~~ 55, ~~56, or 57,~~ wherein the layers in the interband tunnel diode are grown in a chemical vapor deposition (CVD) growth system.

Claim 64. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims ~~54,~~ 55, ~~56, or 57,~~ further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode.

Claim 65 (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims ~~54,~~ 55, ~~56, or 57,~~ further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode, using an inert or reducing atmospheres, or moreover a reduction in ambient gas pressure at a temperature in the range of 300 to 1000°C.

Claim 66. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims ~~54,~~ 55, ~~56, or 57,~~ further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode, using an

inert or reducing atmosphere, or moreover a reduction in ambient gas pressure at a temperature in the range of 450 to 900°C.

Claim 67. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims ~~54,~~ 55, ~~56, or 57,~~ further comprising the step of heat treating the interband tunnel diode, during or after growth of the bottom quantum well layer in the interband tunnel diode.

Claim 68. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims ~~54,~~ 55, ~~56, or 57,~~ further comprising the step of heat treating the interband tunnel diode, during or after growth of the top and bottom quantum well layers, the top and bottom spacer layers, or the tunnel barrier in the interband tunnel diode.

Claim 69. (Original)

The method of fabricating an interband tunnel diode as recited in claim 58, wherein the epitaxial growth system occurs over a substrate temperature range between 50°C and 900°C during growth of the layers in the interband tunnel diode.

Claim 70. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of lowering a substrate temperature before or during growth of the bottom injector layer in the interband tunnel diode.

Claim 71. (Cancelled)

Claim 72. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of elevating a substrate temperature during or after growth of the bottom injector layer in the interband tunnel diode.

Claim 73. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of elevating a substrate temperature during or after growth of the bottom quantum well in the interband tunnel diode.

Claims 74-88. (Cancelled)

Claim 89. (Previously Presented)

A method of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 6 hours.

Claim 90. (Original)

A method of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 1 hour.

Claim 91. (Previously Presented)

A method of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 10 minutes.

Claim 92. (Previously Presented)

A method of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 2 minutes.